a multi-level dielectric layer located over said lower interconnect layer;

an upper m tal interconnect layer located over said multi-level dielectric layer; and

a thin film resistor embedded within said multi-level dielectric layer between and physically separated in a vertical direction from said lower metal interconnect layer and said upper metal interconnect layer.

Please add claims 17 and 18.

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17. An integrated circuit comprising a semiconductor chip that comprises:

a lower metal interconnect layer located over a semiconductor body;

a multi-level dielectric layer located over said lower interconnect layer;

an upper metal interconnect layer located over said multi-level dielectric layer; and

a thin film resistor embedded within said multi-level dielectric layer between said lower metal interconnect layer and said upper metal interconnect layer.

18. The integrated circuit of claim 17, wherein the semiconductor chip further comprises:

a first plurality of conductively filled vias extending from said upper metal interconnect layer to said lower interconnect layer; and

a second plurality of conductively filled vias extending from said upper metal layer to said thin film resistor.